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**Lab 7 Report**

**System-level Design (1)**

**Date \_\_\_\_4/22/17\_\_\_\_\_\_\_**

**by**

**Name \_\_\_\_Anahit Sarao\_\_\_\_\_\_  SID \_\_008435583\_\_\_\_\_\_**

**Name \_\_\_\_Maxwell Cheshier\_\_\_\_\_\_  SID \_\_009193717\_\_\_**

**Lab Record**

|  |  |  |  |
| --- | --- | --- | --- |
| **Tasks** | **Designed by (print name)** | **Verified by (print name)** | **\*Completion Status** |
| **1** | Both | Ryan | A |
| **2** | Maxwell | Ryan | A |
| **3** | Anahit | Ryan | A |

|  |  |  |  |
| --- | --- | --- | --- |
| **Task** | **Performed by (print name)** | **Validated by (print name)** | **\*Completion Status** |
| **4** | **N/A** | **Ryan** | **X** |

**\* Enter the following:**

**A – if the task was successfully completed**

**B – if the task was partially completed**

**X – if the task was failed or not performed**

**If you entered B or X, detailed description about the incompletion or failure must be given in the report.**

**San Jose State University**

**Department of Computer Engineering**

**CMPE 125 Spring 2017**